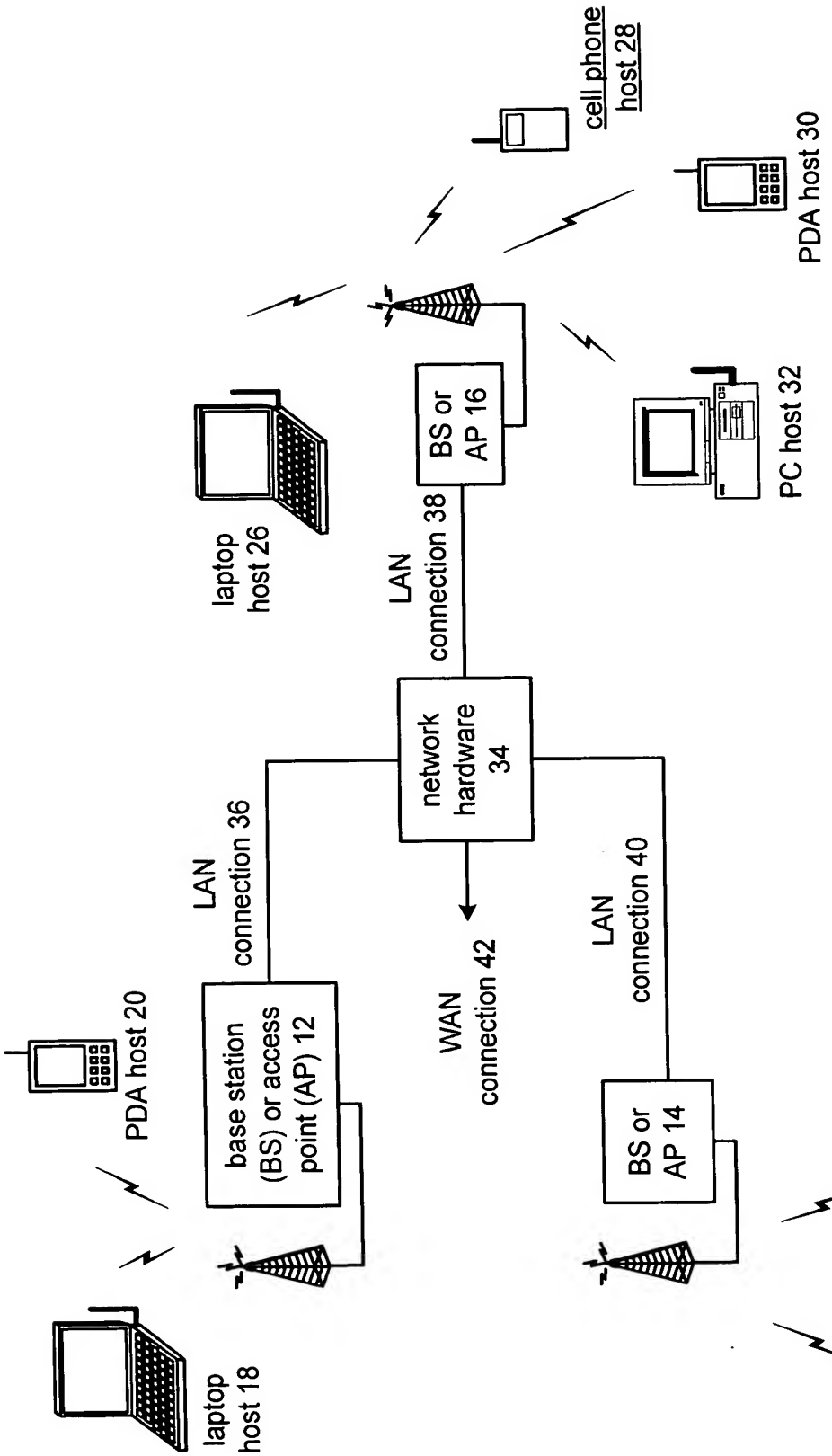

FIG. 1
communications network 10

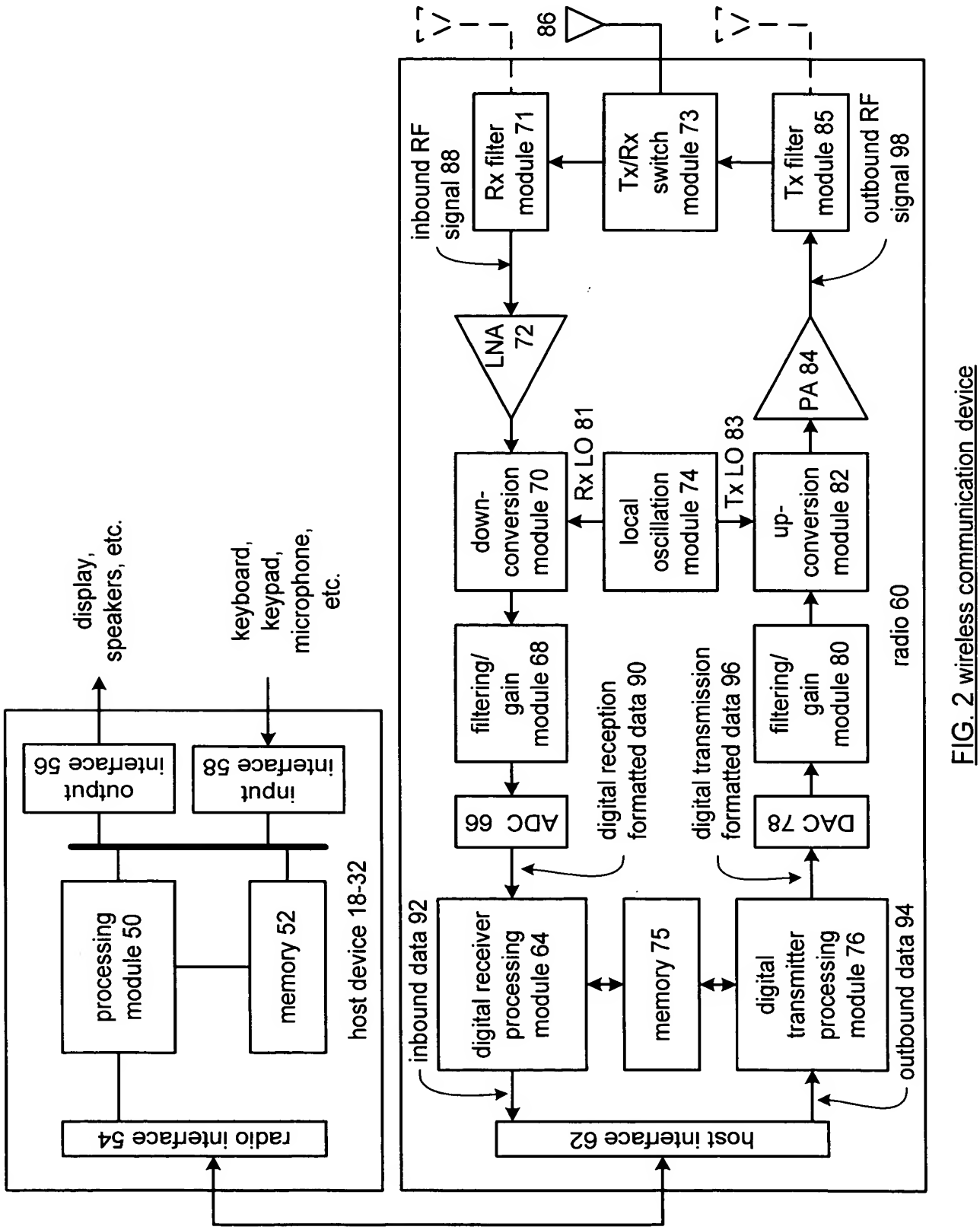

FIG. 2 wireless communication device

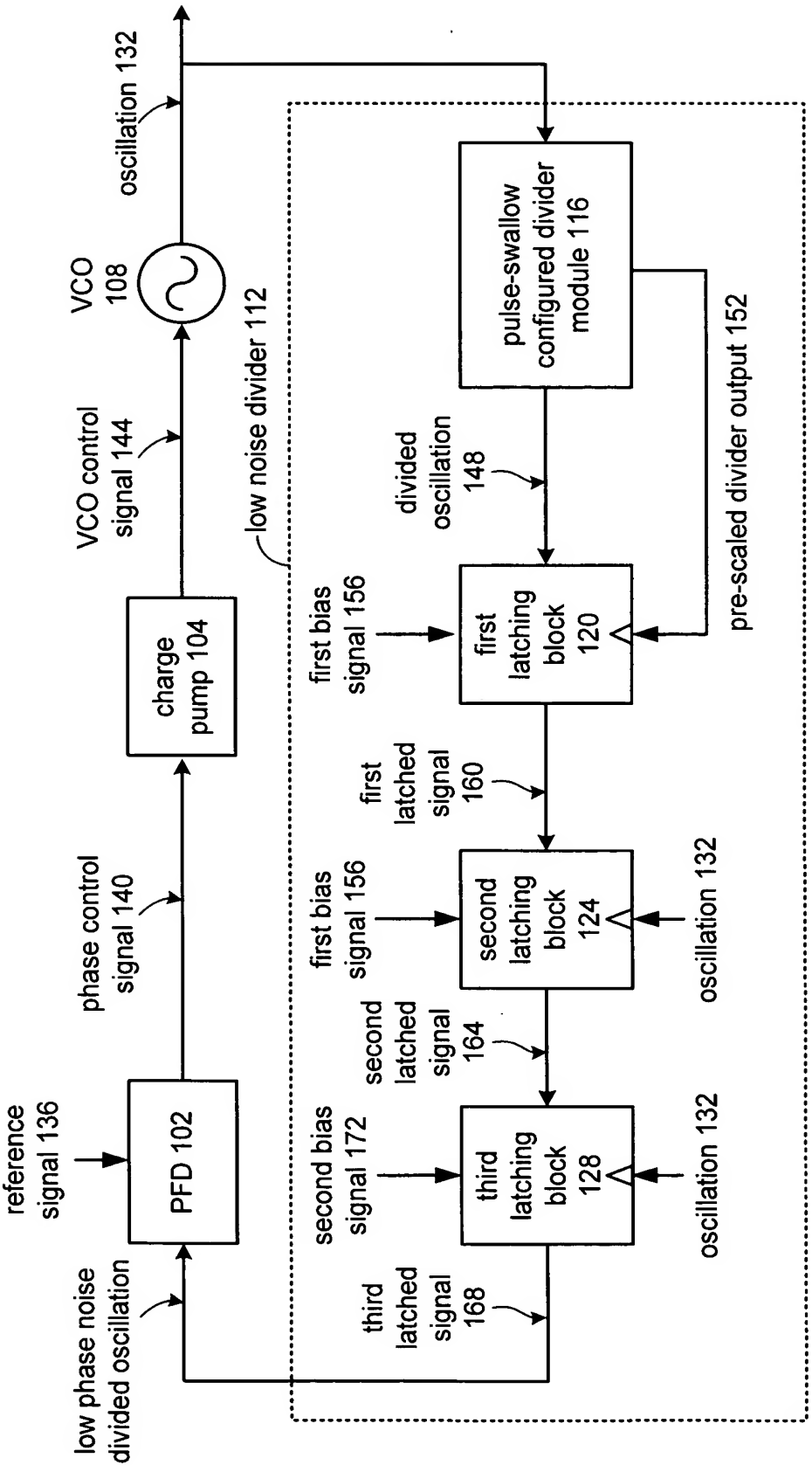

FIG. 3
phase-locked loop 100

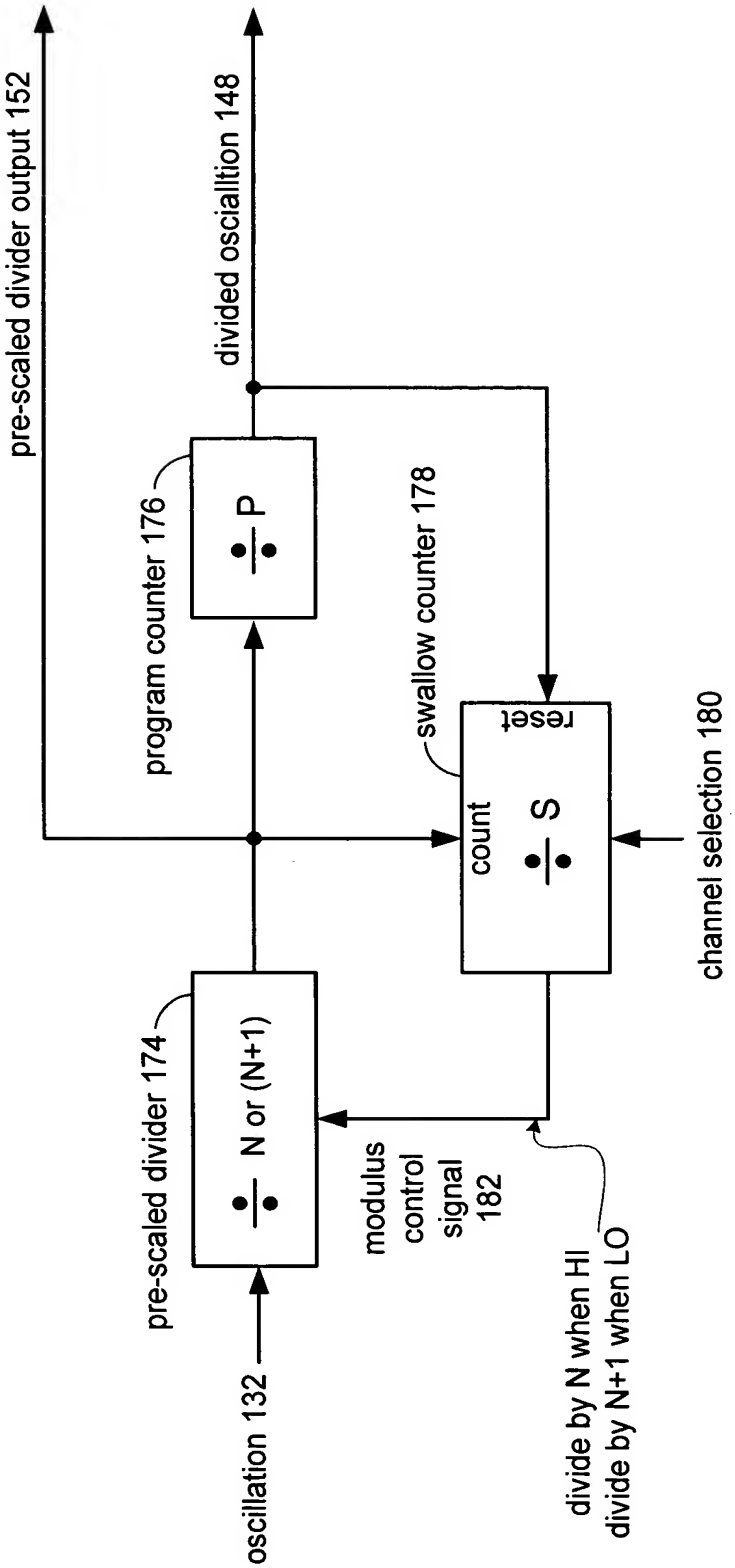

FIG. 4
pulse-swallow configured divider module 116

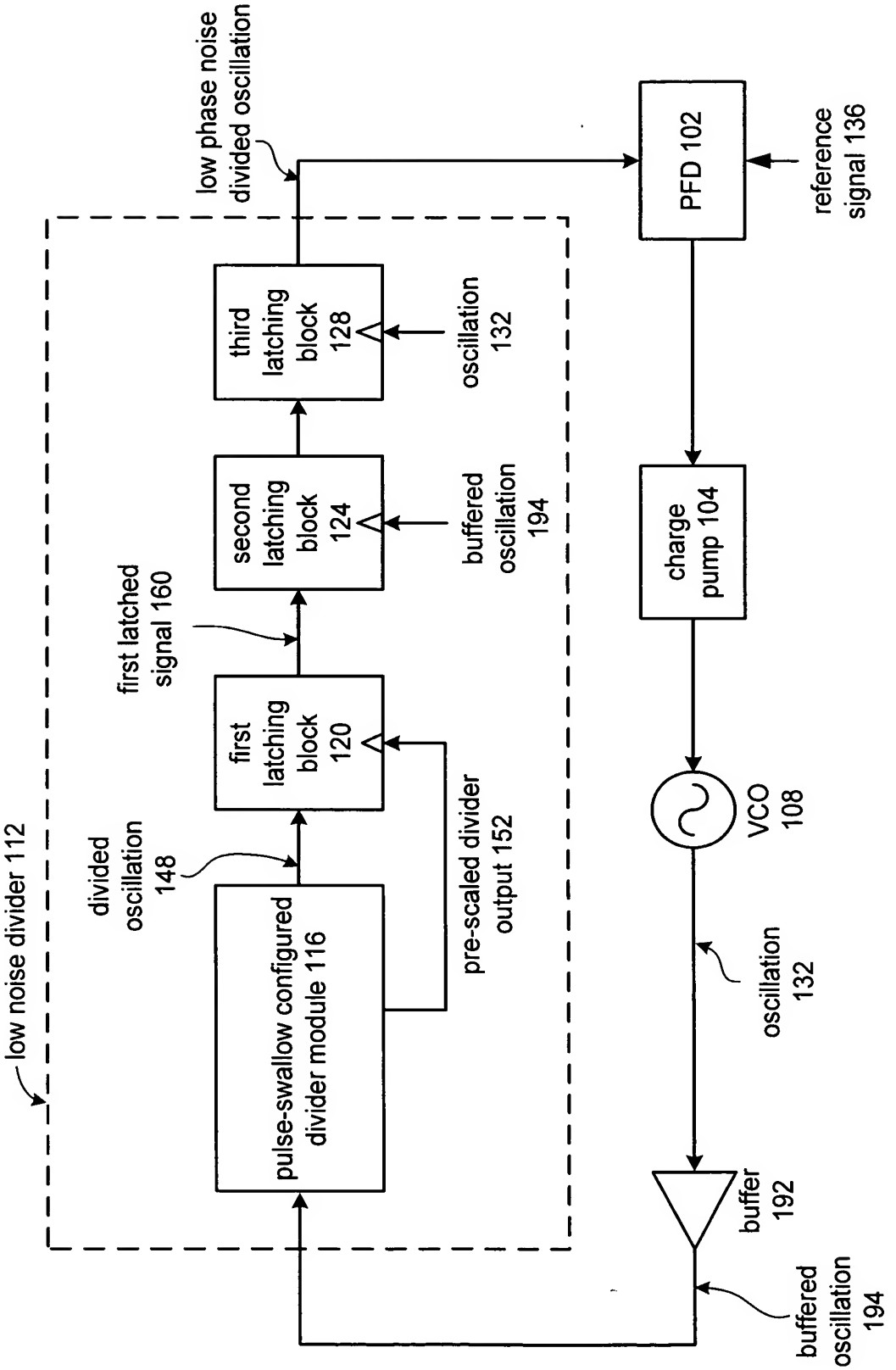

FIG. 5
PLL 100 with buffer

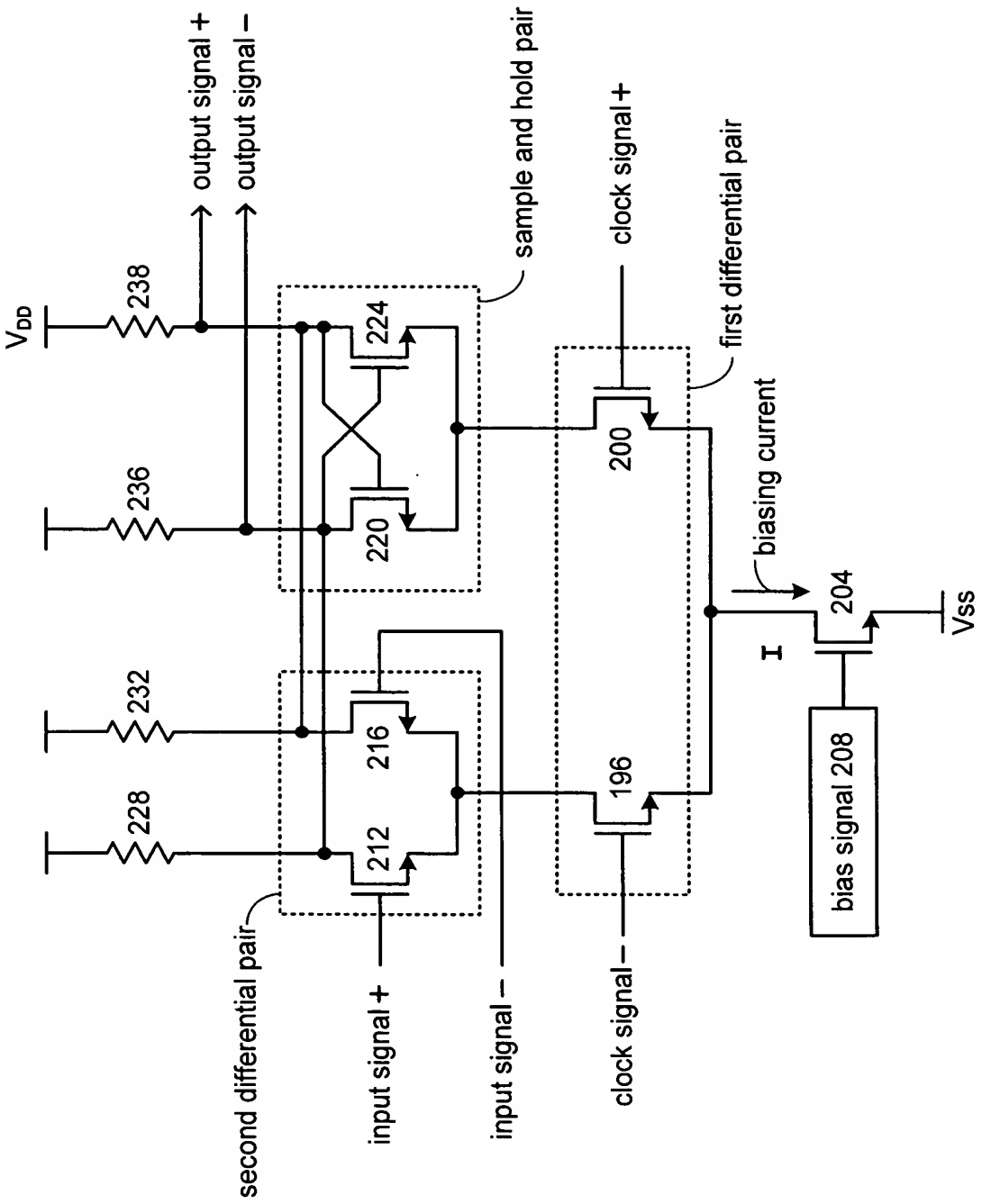

FIG. 6
latching block

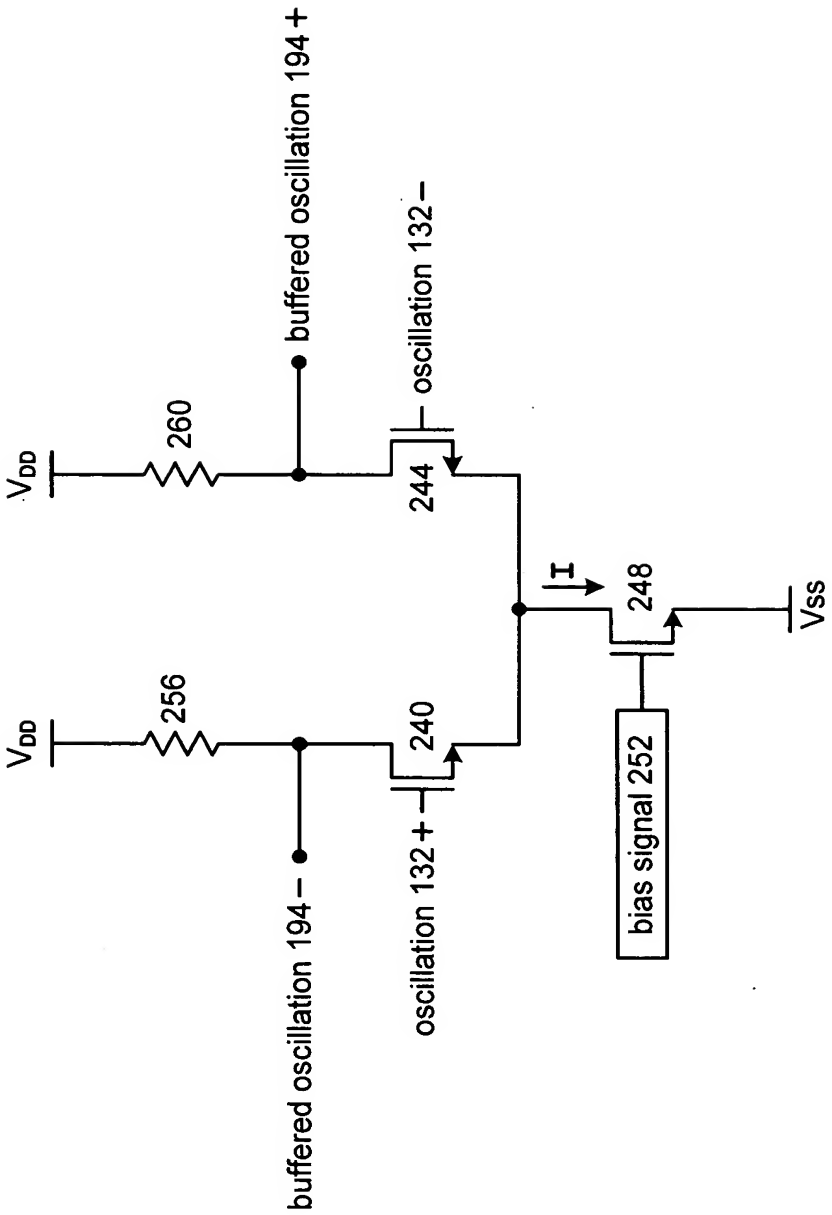

FIG. 7
buffer 192

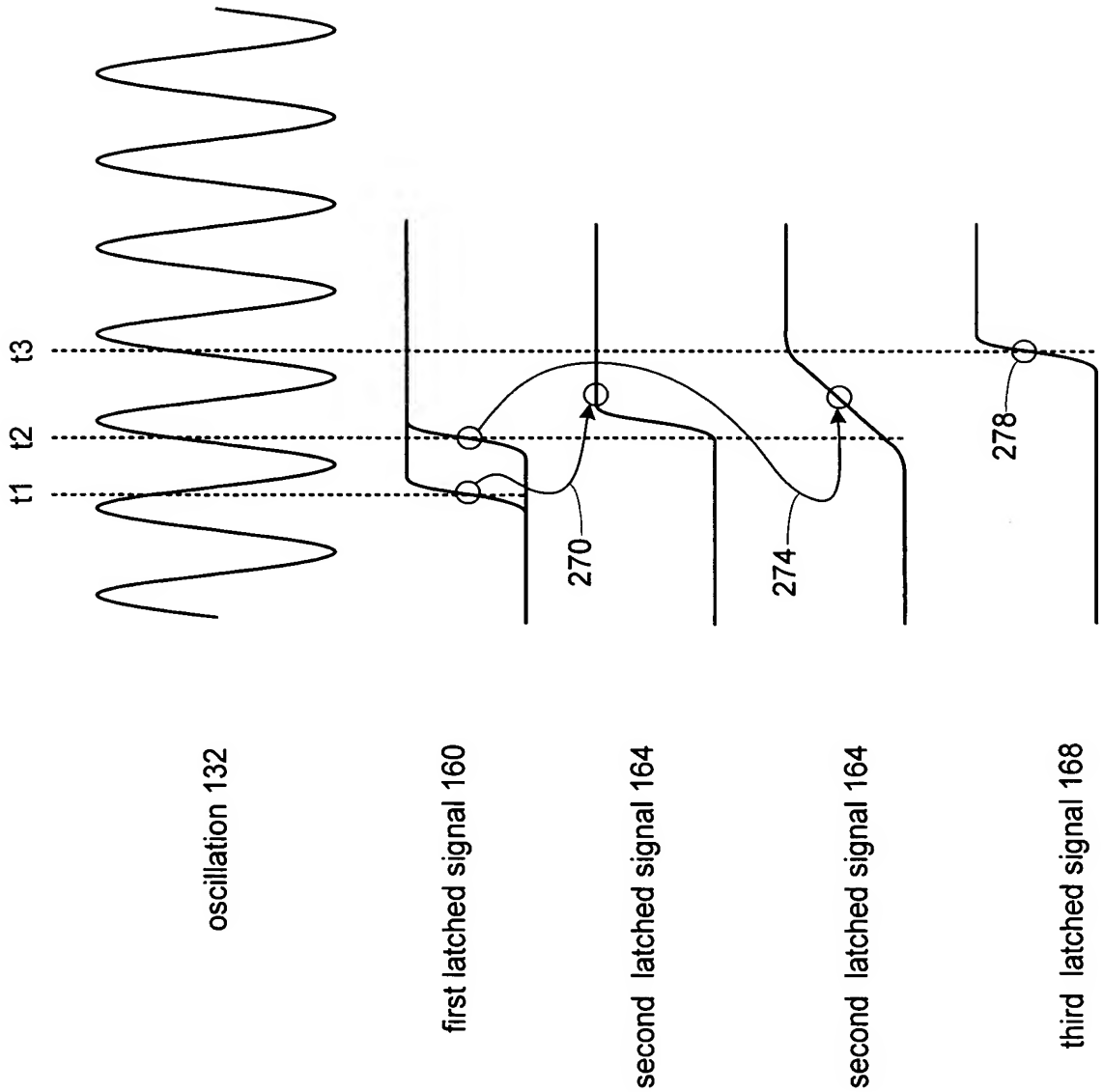

FIG. 8
timing graph

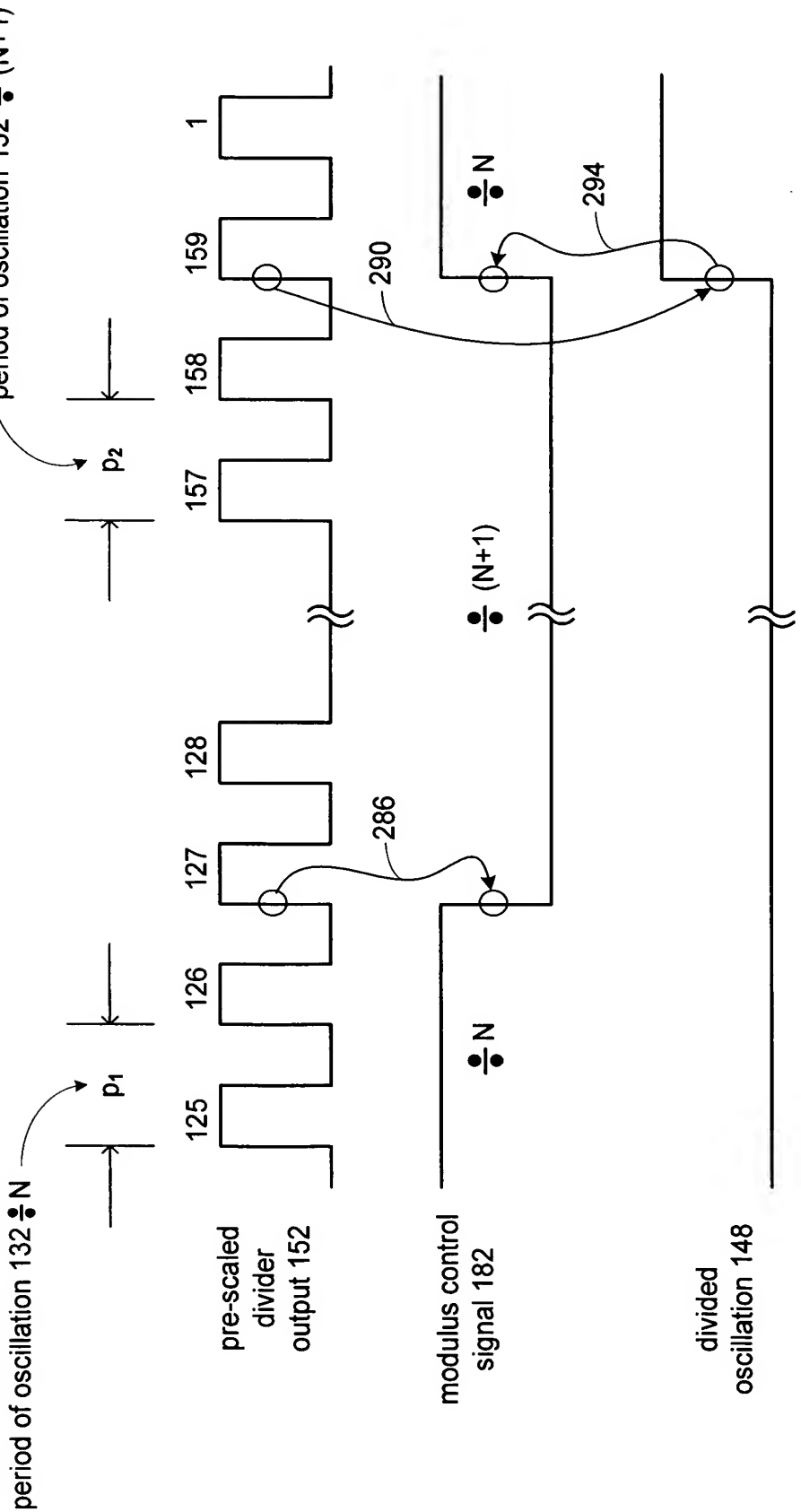

FIG. 9
timing diagrams

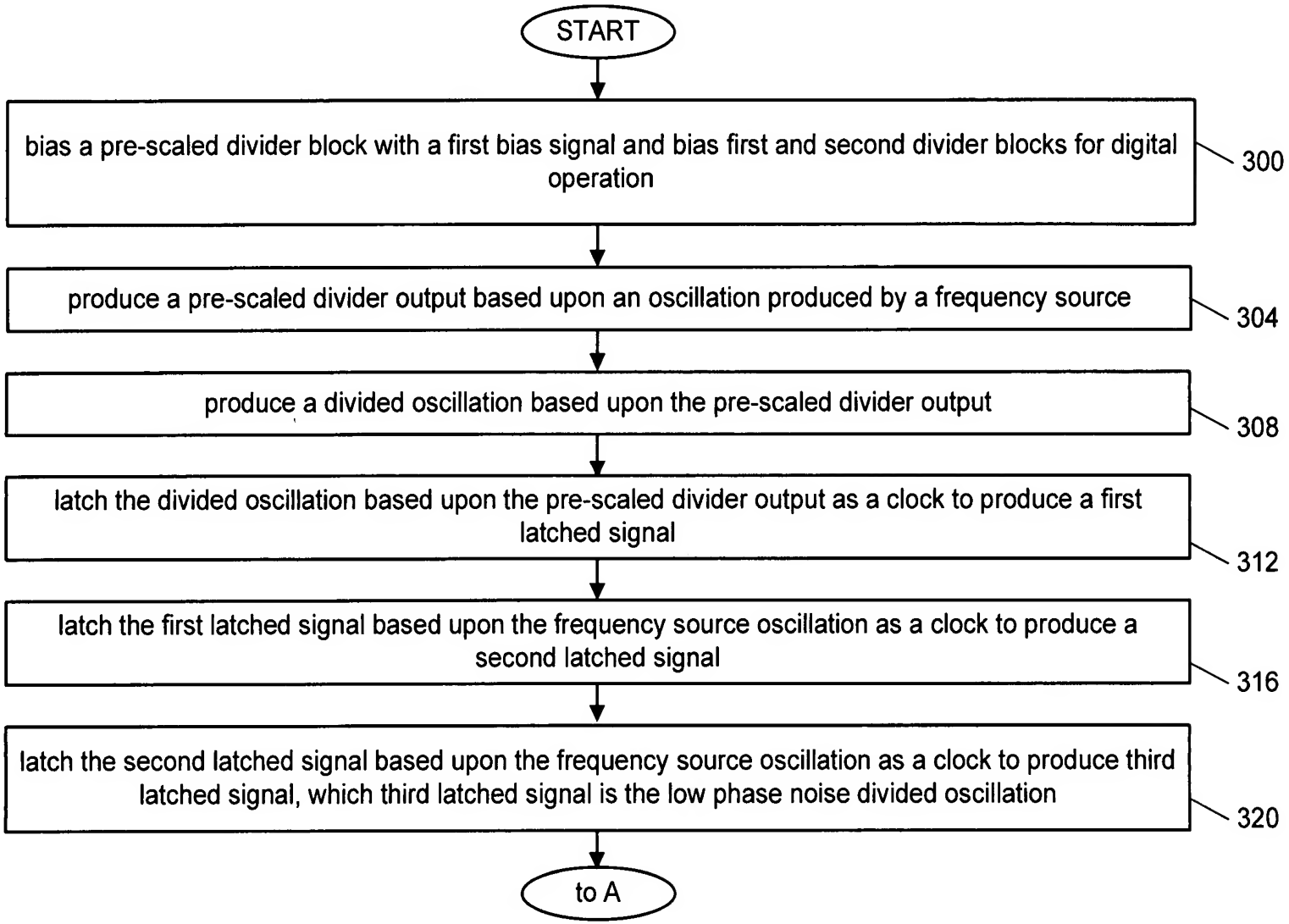

FIG. 10A

method for producing a low phase noise divided oscillation

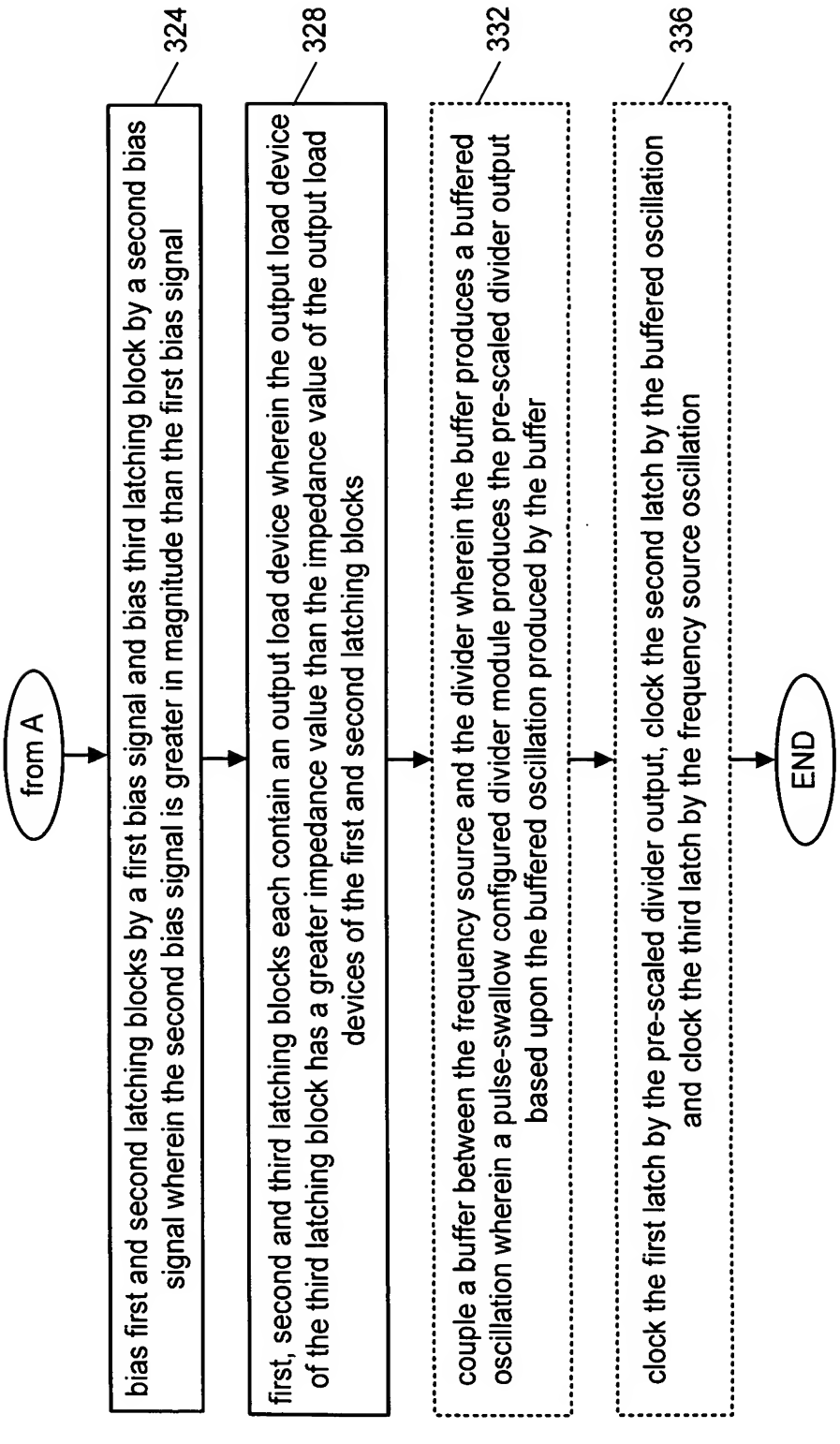

FIG. 10B

method for producing a low phase noise divided oscillation

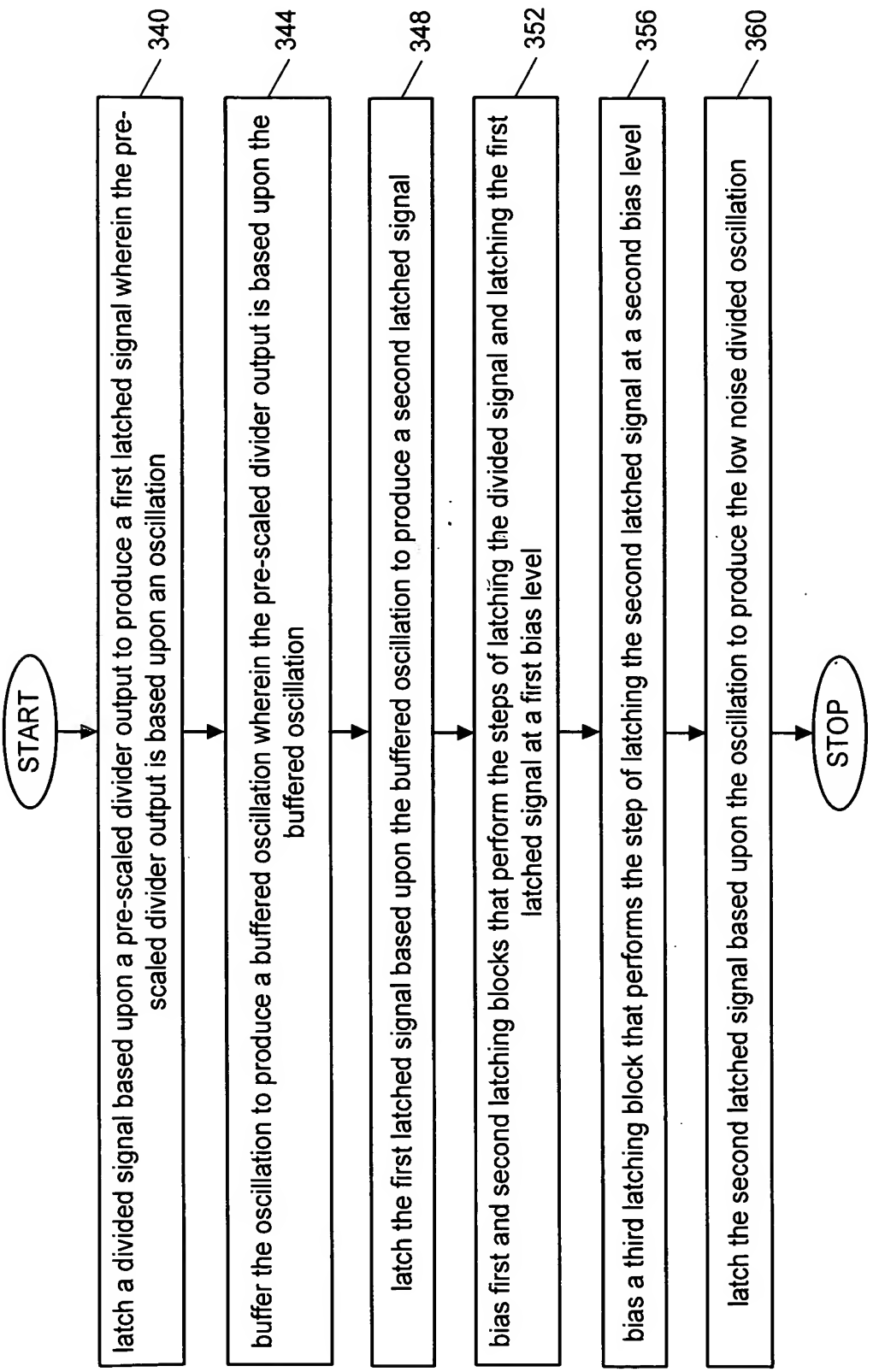

FIG. 11

method for producing a low phase noise divided oscillation